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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,471	09/22/2003	Fumihiko Kato	03FN021US	5531

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EXAMINER	
LUI, DONNA V	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 11/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/665,471	KATO, FUMIHIKO	
	Examiner	Art Unit	
	Donna V. Lui	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,7,8,13-15 and 17-20* is/are rejected.

7)☐ Claim(s) *3-6,9-12 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/19/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. **Claims 1, 3, 5, 18, and 19** are objected to because of the following informalities: The following claims were interpreted as follows. Appropriate correction is required.

Claim 3, line 9: plurality of voltage output terminals that constitute ~~constituting~~ the associated reference-voltage output

Claim 3, line 11: voltage output terminal group, the ~~that~~ reference-voltage output terminal which

Claim 3, line 14: an operational amplifier having a positive input ~~output~~ terminal to which an output of said

Claim 3, line 15: reference voltage selector is input, a negative input ~~output~~ terminal connected to said first terminal

Claim 5, line 2: of said node selector includes a plurality of switches having ~~one~~ ends connected together to

Claim 5, lines 4-5: output terminals of the associated reference-voltage output terminal group and enables the ~~that one of said~~ switches which are ~~is~~ selected based on said correction adjustment data.

Claim 6, line 3: a first switch circuit including a plurality of switches having ~~one~~ ends connected

Claim 6, line 8: circuit and having ~~one~~ ends connected together to said second terminal and other ends

Claim 18, line 2: circuit of said node selector includes a plurality of switches having ~~one~~ ends connected

Claim 18, line 5: enables the ~~that one of said~~ switches which are ~~is~~ selected based on said correction adjustment data.

Claim 19, line 3: a first switch circuit including a plurality of switches having ~~one~~ ends connected

Claim 19, line 8: circuit and having ~~one~~ ends connected together to said second terminal and other ends

Claim 19, line 10: enables the ~~that one of said~~ switches of the first switch circuit which are ~~is~~ selected based on

Claim Rejections - 35 USC § 112

2. **Claim 17** recites the limitation "said reference voltage selector" and "said data latch" in lines 1-3. There is insufficient antecedent basis for this limitation in the claim.

3. **Claim 18** recites the limitation "said switch circuit", "said node selector", "said first terminal" and "said second terminal" in lines 1-3. There is insufficient antecedent basis for this limitation in the claim.

4. **Claim 19** recites the limitation "said first terminal" and "said second terminal" in lines four and eight respectively. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. **Claims 1-2, 7-8, 13-15 and 17-20** are rejected under 35 U.S.C. 102(b) as being anticipated by Nitta et al. (Pub. No.: US 2002/0011979 A1).

With respect to **Claim 14**, A display panel drive apparatus *(See figure 1)* comprising: a data-line drive circuit *(element 7-1, 7-2, ..., 7-8)* provided with a gray voltage *(element 26 provides gray voltage from element 15)*; and a gamma correcting circuit *(elements 11 and 13 provide signals to element 15 in accordance with gamma coefficients)* in electrical

communication *(note that the gamma correcting circuit is within the data-line drive circuit)* with the data-line drive circuit providing the gray voltage and comprising:

a basic voltage generating circuit *(See figure 1; See figure 5: element 15 of figure 1; See figure 6: circuit of elements 201-1, 203-1, and 205-1 of figure 5, element 201: basic voltage generating circuit)* which has one end connected to a first high-potential power supply *(See figure 5 and figure 6, first high-potential power: VS0)* and the other end connected to a first low-potential power supply *(See figure 5 and figure 6, first low-potential power: VS255)* and generates and outputs a plurality of basic voltages by dividing a voltage difference between a voltage of the first high-potential power supply and a voltage of the first low-potential power supply *([0060], lines 5-13)*; a gamma correction resistor circuit *(See figure 6, element 205)* having a plurality of resistor elements connected in series between a second high-potential power supply *(See figure 6, element VG0)* and a second low-potential power supply *(See figure 6, element VG255)*, and gray-scale voltage output terminals and n (n being a positive integer greater than one) reference-voltage output terminal groups *(See figure 5, elements 204-1 and 204-2; note that n=2 being elements 204-1 and 204-2)*, both provided at respective nodes between the resistor elements *(See figure 6, note that figure 6 is a circuit representation of positive reference voltage for elements 201-1, 202-1, 203-1, 204-1, and 205-1 of figure 5 and are similarly applied to negative reference voltage for elements 201-2, 202-2, 203-2, 204-2, and 205-2 of figure 5)*, each of the n reference-voltage output terminal groups including a maximum of u (u being a positive integer greater than one) reference-voltage output terminal candidates *(See figure 6, VG0, VG1, ..., VG255: reference-voltage output terminal candidates, u=256)*; and a gamma correction adjusting circuit *(See figure 6, element 203)* having n gamma characteristic adjusting

units *(note that figure 6 is a circuit representation for positive reference voltages and negative reference voltages are similarly applied, thus there are two gamma characteristic adjusting units)* in association with the n reference-voltage output terminal groups, each of which selects one of a maximum v (v being a positive integer greater than one) basic voltages *(See figure 6, VS0, VS1, ..., VS255: basic voltages, v=256)* supplied from the basic voltage generating circuit as a reference voltage based on correction adjustment data *([0053], lines 1-4; [0060], lines 5-13)* and selects *(See figures 7 and 8; [0063])* an output terminal for the selected reference voltage from the maximum of u reference-voltage output terminal candidates included in the associated one of the n reference-voltage output terminal groups based on the correction adjustment data *(See figure 7, element 14)*.

With respect to **Claim 1**, Claim 1 is a gamma correcting circuit, whereas Claim 14 is a display panel drive apparatus comprising the limitations of claim 1. Thus Claim 1 is analyzed as previously discussed with respect to Claim 14.

With respect to **Claims 2 and 15**, the display panel drive apparatus according to claims 14 and 1 respectively, Nitta teaches the basic voltage generating circuit *(See figure 6, element 201)* has a plurality of resistor elements connected in series between the first high-potential power supply *(element V0 is equivalent to VS0)* and the first low-potential power supply *(element V8 is equivalent to VS255)* and outputs individual basic voltages *(elements VS0, VS1, VS2, ..., VS254, VS255)* from nodes between those resistor elements.

With respect to **Claim 7**, Nitta teaches a display panel drive apparatus *(See figure 1)* having a gamma correcting circuit as recited in claim 1.

With respect to **Claim 8**, Nitta teaches a display panel drive apparatus *(See figure 1)* having a gamma correcting circuit as recited in claim 2.

With respect to **Claims 20 and 13**, the display panel drive apparatus according to claims 14 and 1 respectively, Nitta teaches the first and second low-potential power supplies supply power greater than zero *([0059], lines 1-8; note that since the voltages V0-V8 represent positive gray scale voltages than the supply power is greater than zero).*

With respect to **Claim 17**, the display panel drive apparatus according to claim 15, Nitta teaches a reference voltage selector *(See figure 6, element 206)* selects a reference voltage based on a first predetermined portion of the correction adjustment data *(See figure 9, the gray scale control register includes 10 six bit registers, the first bit register (No 1) is a first predetermined portion; [0064], lines 6-8)* latched by the data latch and a node selector *(See figure 6, element 207; See figures 7 and 8)* selects a reference-voltage output terminal based on a second predetermined portion of the correction adjustment data *(See figure 9, the second bit register (No 2) is a second predetermined portion).*

With respect to **Claim 18**, the display panel drive apparatus according to claim 15, Nitta teaches a switch circuit of a node selector *(See figure 6, element 207; See figures 7 and 8)*

includes a plurality of switches having ends connected together to a first terminal *(See figures 7 and 8, wiring connected to V0 and V8)* and a second terminal *(See figures 7 and 8, wiring connected to B1, B2, ..., B6 and W6, W7, ..., W1)* and other ends connected to respective voltage output terminals *(See figures 7 and 8; VG8, VG16, VG24, ..., VG56; VG200, VG208; VG216, ..., VG248)* of the associated reference-voltage output terminal group *(the reference-voltage output terminal group being the group having positive reference voltages supplied by element 8)* and enables that one of the switches which is selected based on the correction adjustment data *(See figure 9, note that if RS = '0' then the switches in connection with the outputs B1, ..., B6 and W1, ..., W6 are enabled).*

With respect to **Claim 19**, the display panel drive apparatus according to claim 15, where the node selector *(See figure 6, element 207; See figures 7 and 8)* has: a first switch circuit *(See figure 7, element 207)* including a plurality of switches having ends connected together to a first terminal *(See figure 7, wiring connected to V0)* and other ends connected to respective voltage output terminals of the associated reference-voltage output terminal group *(See figure 7; wiring connected to B1, B2, ..., B6; VG8, VG16, VG24, ..., VG56: voltage output terminals)*; and a second switch circuit *(See figure 7, element 208)* including a plurality of switches provided in association with the switches of the first switch circuit *(note that switches are provided in association with the switches of the first switch due to the dependency of the correction adjustment data; See figure 9, note that when RS = '0' switches in both the first switch circuit and second switch circuit are enabled)*, equal in number to the switches of the first switch circuit *(number of elements of B1, ..., B6 = number of elements of W1, ..., W6)* and having ends

connected together to a second terminal *(See figure 7, wiring connected to V8)* and other ends respectively connected to the other ends of the switches of the first switch circuit *(note that the connection of the other ends of the second switch circuit to the other ends of the first switch circuit is wiring and resistors common to the voltage output terminals)*, and enables that one of the switches of the first switch circuit which is selected based on the correction adjustment data and that one of the switches of the second switch circuit which is associated with the selected switch *(See figure 9, note that switches in both the first switch circuit and the second switch circuit, are enabled when RS= '0')*.

Allowable Subject Matter

7. **Claims 3-6, 9-12, and 16** would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

With respect to **Claims 3 and 16**, the display panel drive apparatus according to claim 14, Nitta teaches each of the gamma characteristic adjusting units includes: a data latch *(See figure 1, element 13)* which fetches and latches correction adjustment data at a predetermined timing; a reference voltage selector *(See figure 6, element 206)* which receives a plurality of basic voltages and selects and outputs one of the basic voltages as a reference voltage based on the correction adjustment data *(See figure 6, element 14)* latched by the data latch; a node selector *(See figures 7 and 8, elements 207 and 208 respectively)* which has a first terminal *(wiring connected to V0 and V8)*, a second terminal *(wiring connected to B1, B2, ..., B6 and W6,*

W7, ..., W1), a switch circuit (See switches between first and second terminals in figures 7 and 8) and a plurality of voltage output terminals (B1, B2, ..., B6 and W6, W7, ..., W1) that constitute the associated reference-voltage output terminal group and selects, from the voltage output terminal which is connected to the first terminal and the second terminal by the switch circuit, based on the correction adjustment data latched by the data latch.

None of the prior art teaches the above with an operational amplifier having a positive output terminal to which an output of the reference voltage selector is input, a negative output terminal connected to the first terminal and an output terminal connected to the second terminal.

Response to Arguments

8. Applicant's arguments filed 8/31/2006 have been fully considered but they are not persuasive.

Applicant argues that "groups" and "candidates" are plural integers and have been defined as such.

The examiner respectfully disagrees. The claim limitation recites "(u being a positive integer)", which is inclusive of the number one. Please note that a group is a set and a set is a collection of numbers, where a set can have zero numbers, thus a group can consist of one number being equivalent to a candidate. Please further note that "groups" and "candidates" were not defined as plural integers until applicant's amendment submitted on 8/31/2006.

9. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donna V. Lui whose telephone number is (571) 272-4920. The examiner can normally be reached on Monday through Friday 8:30 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571)272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Donna V Lui
Examiner
Art Unit 2629

AMR A. AWAD
SUPERVISORY PATENT EXAMINER